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LAP-D protocol implementation for a PC-based ISDN central office

Suresh Dongre
Iowa State University

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by

Suresh Dongre

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CHAPTER 1. INTRODUCTION

For more than a century, the primary communication system has been the telephone system. It had been solely intended for analog voice traffic. But with the rapid advances in computer and communication technologies, the current communication system is proving inadequate for modern communication needs like data transmission, video, and facsimile. User demands for these and other services have led to an international undertaking to replace a major portion of the worldwide telephone system with an advanced digital system. The new system, called **Integrated Services Digital Network (ISDN)**, has its objective of integrating voice and non voice traffic over a single network. CCITT (International Telegraph and Telephone Consultative Committee), the organization that establishes global standards for telecommunication, soon took an active role in developing standards for ISDN. The CCITT I-series Preamble refers to ISDN as a network "that provides end to end digital connectivity to support a wide range of services by a limited set of standard multipurpose user network interfaces." To realize the ISDN objective, the existing network has to be modified.

The first section briefly discusses the various services provided by ISDN. The second section looks at the user interface to the ISDN. The third section introduces the concept of central office and the functions associated with it. Finally, the orga-

nization of the thesis is detailed.

ISDN Services

ISDN provides various services, supporting existing applications of voice and data, alongwith other new applications. On a broad perspective, ISDN services can be categorized under voice, data, text, and image (refer Table 1.1). Most of these services can be realized with a transmission capacity of 64 kbps. However, applications like High definition Television etc., require larger channel capacity outside the scope of the existing ISDN.

A new revolutionary concept has evolved to overcome the above problem. It is referred to as Broadband ISDN (B-ISDN). With technological advances in the areas of optical fibre communication and high-quality video monitors and cameras, the B-ISDN integrates a wide range of communication facilities to form a universal communication with the following key characteristics [1]:

- Worldwide exchange between any two subscribers in any medium or a combination of media.
- Retrieval and sharing of massive amounts of information from multiple sources, in multiple media, among people in a shared electronic environment.
- Distribution, including switched distribution, of a wide variety of cultural, entertainment, and educational materials to home or office, virtually on demand.

Table 1.1: Services supported by ISDN

Services			
Telephony	*Data*	*Text*	*Image*
Telephone	Packet-switched data	Telex	
	Circuit-switched data	Teletex	
Leased circuits	Leased circuits	Leased Circuits	
	Telemetry	Videotex	
	Funds transfer		Facsimile
	Mailbox	Mailbox	Surveillance
	Electronic mail	Electronic mail	
	Alarms		
Music	High speed computer		TV conferencing
	communication		
			Teletex
			Videophone
			Cable TV distribution

Central Office

In any communication system connecting several users, different protocols may be adopted to connect one user to another. A typical communication network is shown in Figure 1.1. User A can be connected to user B either by a dedicated path or by a virtual path (wherein any available channel is used for transfer). The former method, called circuit switched service, is reliable but expensive. The latter is not very efficient but economical. The tradeoff is based on the type of information transfer. In a telephone system where accurate information transfer is very vital,

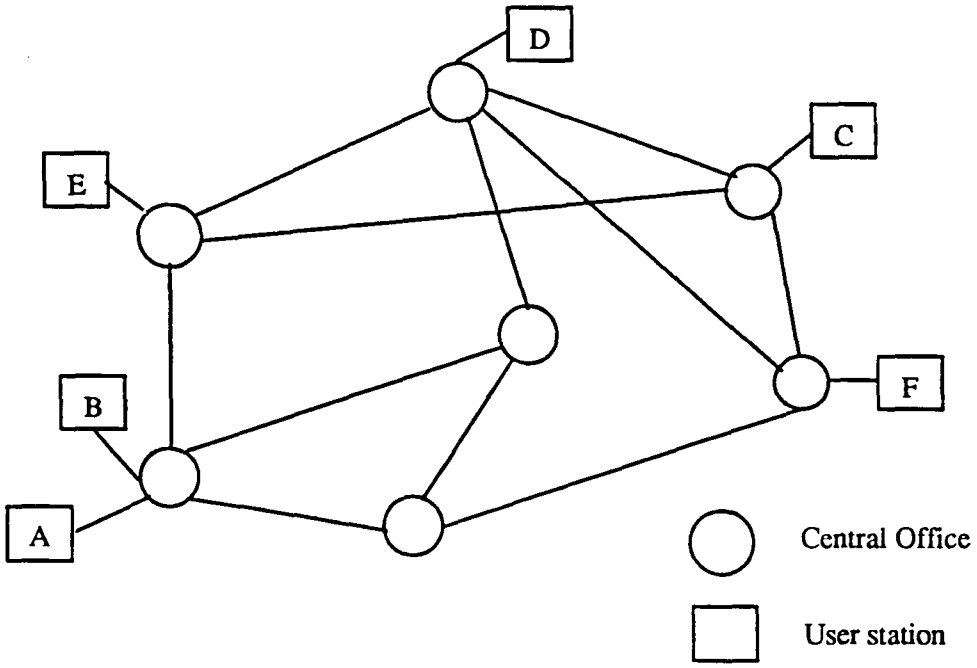


Figure 1.1: A typical communication network

connection oriented mechanism is employed. ISDN employs the circuit switched service. If user A wishes to place a call to user B, then the central office connecting A and B switches the line of A to that of B thereby establishing a physical connection. On the other hand, if user A wishes to place a call to user C (outside the scope of the central office of A), then the central office of A has to find a *route* between A and C and switch the call accordingly i.e switch the call eventually to the central office connecting C.

Thus, a central office primarily deals with:

- Switching
- Routing

The objective of this research is to realize an ISDN Central Office for a laboratory

environment. Three graduate students have been involved in developing the hardware for the central office which include:

1. S/T Interface card
2. U Interface card
3. Switch card

User Interface

Figure 1.2 shows a conceptual view of ISDN from the user point of view. Any user interfaces to the ISDN through a "digital pipe" of a certain bit rate. The user equipment can be any of the existing non-ISDN type like telephone, LAN, data terminal, or an ISDN type like a digital PBX with local switching capabilities.

At any given time, the pipe can have a variable mix of traffic, but the capacity of the pipe is fixed. Thus, a user may access circuit switched, packet switched, or a dynamic mix of signal types as depicted in Figure 1.2.

Organization of the Thesis

In this thesis I have implemented the Layer 2 protocol for D-channel (LAP - D) in accordance with the CCITT Q.921 specifications. The thesis has been organized into the following chapters:

Chapter 2 provides a general description of the ISDN transmission structure, the architecture, and the various protocols. Chapter 3 looks into the hardware design of the Central Office. Chapter 4 discusses the layer 2 software implementation on the

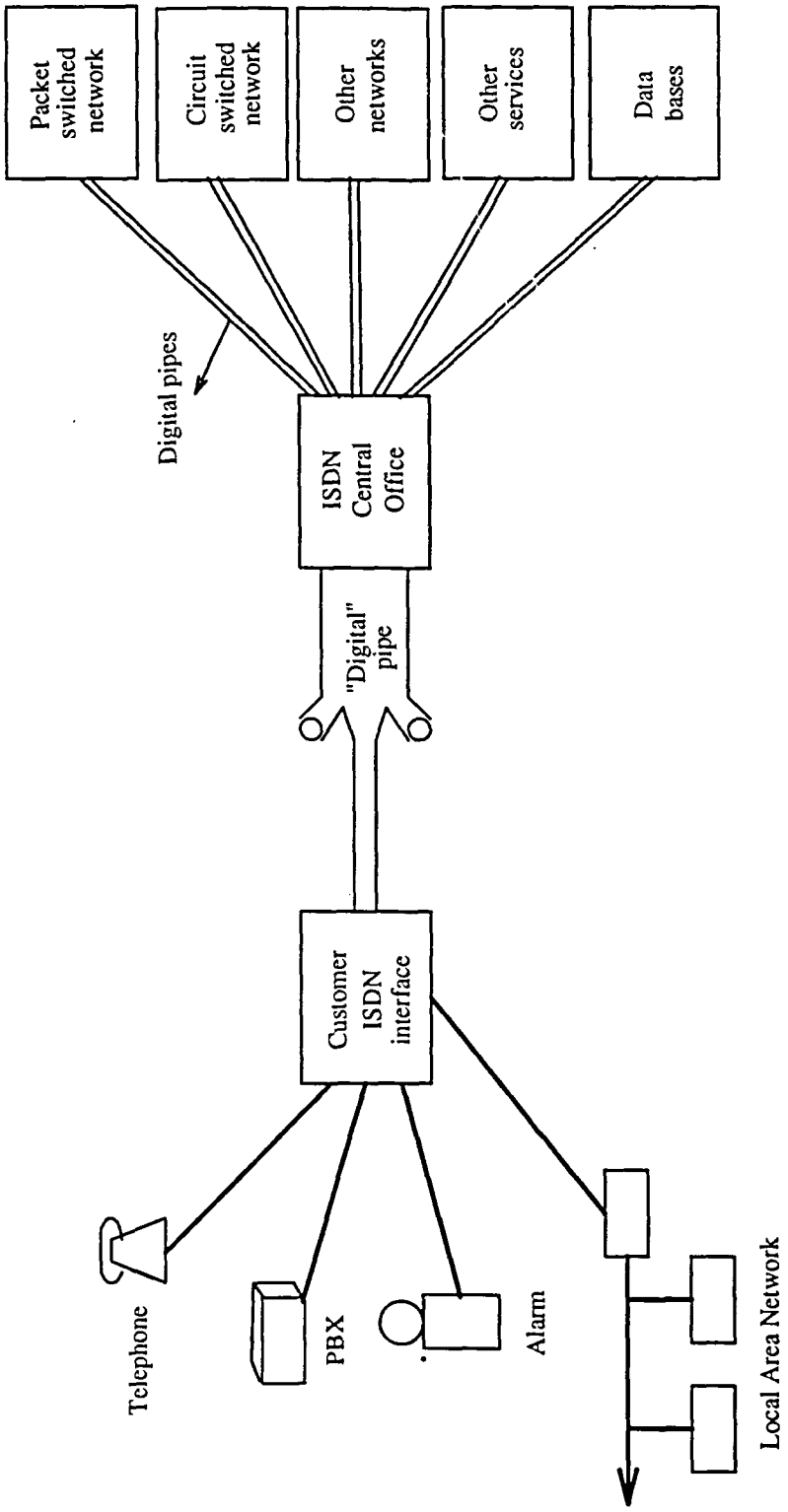


Figure 1.2: Conceptual view of ISDN connection

S/T interface. LAP-D, Interrupt routines and other key aspects of software design are addressed. Finally, conclusions reached from this research are in Chapter 5.

CHAPTER 2. ISDN - AN OVERVIEW

In this chapter, the key network aspects required to realize ISDN, the architecture and channel structures, and some of the protocols are discussed.

Transmission structure

The user interfaces to the ISDN through a conceptual "digital pipe." Information transfer (analog/digital) takes place through this pipe in both directions. Further, with time division multiplexing, this digital pipe supports independent multiple channels. The capacity of the pipe, and thus the number of channels, varies from user to user depending upon the service requirement. Standards have been developed for defining this capacity by assigning the following types of channels:

- B channel: 64 kbps
- D channel: 16 kbps
- H channel: 384, 1536, or 1920 kbps

The B-channel is used to carry digitized traffic like digital data, PCM encoded voice, and a mixture of both. Consequently, two types of connections can be set up over this channel:

- Circuit switched

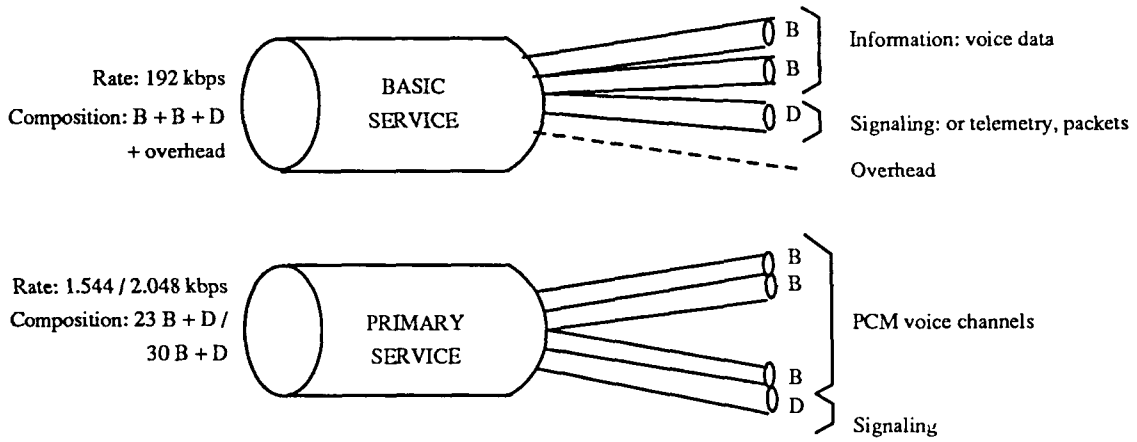


Figure 2.1: ISDN transmission standards

- Packet switched

The D-channel is mainly used for control signalling during the setup of a connection. It can also be used for lower rate digital traffic.

The H-channel is used for very high data rate traffic like facsimile, video etc.

There are two standards that define the bandwidth of the digital pipe (see Figure 2.1):

- Basic Service, for domestic use, with a channel capacity of 2B + D i.e. 192 kbps, including transmission overhead.
- Primary Service, for commercial use such as offices with PBX or a LAN, with a channel capacity of 23B + D/30B + D i.e. 1.544 kbps/2.048 kbps, including transmission overhead.

The primary transmission standard has been developed to correspond to the existing T1 transmission facility of AT&T. This makes the evolution of ISDN from the present telephone system faster, and with minimal overhead.

ISDN System Architecture

A conceptual ISDN architecture for domestic use is shown in Figure 2.2 [2]. Based on the functionality and location of the user equipment, CCITT defines the architecture using:

- Functional Groupings: Certain arrangement of user equipment providing a specific service(s).
- Reference Points: Conceptual points separating the functional groupings.

There are four types of functional groupings:

- Network Termination 1 (NT1)
- Network Termination 2 (NT2)
- Terminal Equipment 1 (TE1)
- Terminal Equipment 2 (TE2)

The functions of NT1 are associated with the physical and electrical termination of the ISDN equipment on the users premises. This separates the user from the actual transmission technology. It has a connector onto which an ISDN cable can be inserted. Up to 8 ISDN devices can be connected to the cable. This implies that, at any instance, all these equipment may wish to access the D-channel. Consequently, contention resolution algorithms are provided to access the D-channel. Further, NT1 contains electronics for network administration, maintenance, local and remote loopback testing, and performance monitoring. The functions of NT2 are very similar to that of NT1. The additional functions include capability of switching calls within

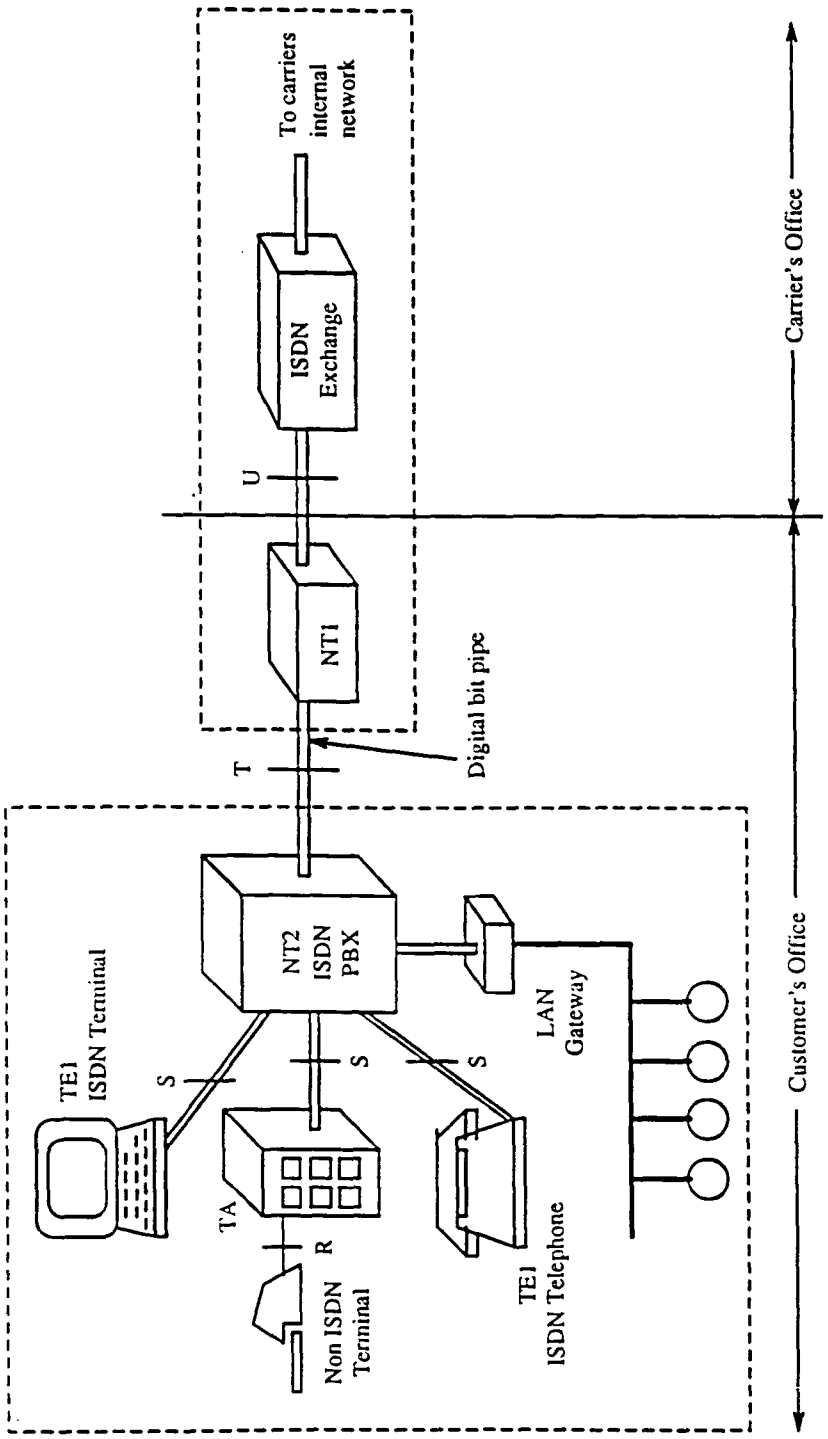


Figure 2.2: Conceptual ISDN architecture

user premises, and support of more than 8 ISDN terminals. A typical example of NT2 is the digital PBX.

Terminal equipment 1 (TE1) are standard ISDN equipment which support the ISDN transmission format. Examples of this include digital telephone, integrated voice/data terminal etc.. Terminal equipment 2 (TE2) are the existing non-ISDN equipment that support transmission protocols like RS-232, X.25 etc.. These equipment however, can be integrated with TE1 through a terminal adaptor which converts TE2 for an ISDN interface.

As mentioned earlier, reference points are those conceptual points that delimit the above functional groupings. CCITT defines the following reference points:

- R: this separates the terminal adaptor and TE2
- S: this separates NT2 and TE1/TA
- T: this separates NT2 and NT1
- U: this separates NT2 and the local ISDN exchange

ISDN Protocols

In order to define the ISDN protocols, it is imperative that an analogy be drawn between ISDN and the OSI layered architecture. Figure 2.3 suggests a relationship between the two.

From the user-network interface standpoint, ISDN is unconcerned with layers 4-7 which pertain to internetworking and thus beyond the user premises. Since the B and D-channel are multiplexed over a single transmission conduit, the physical

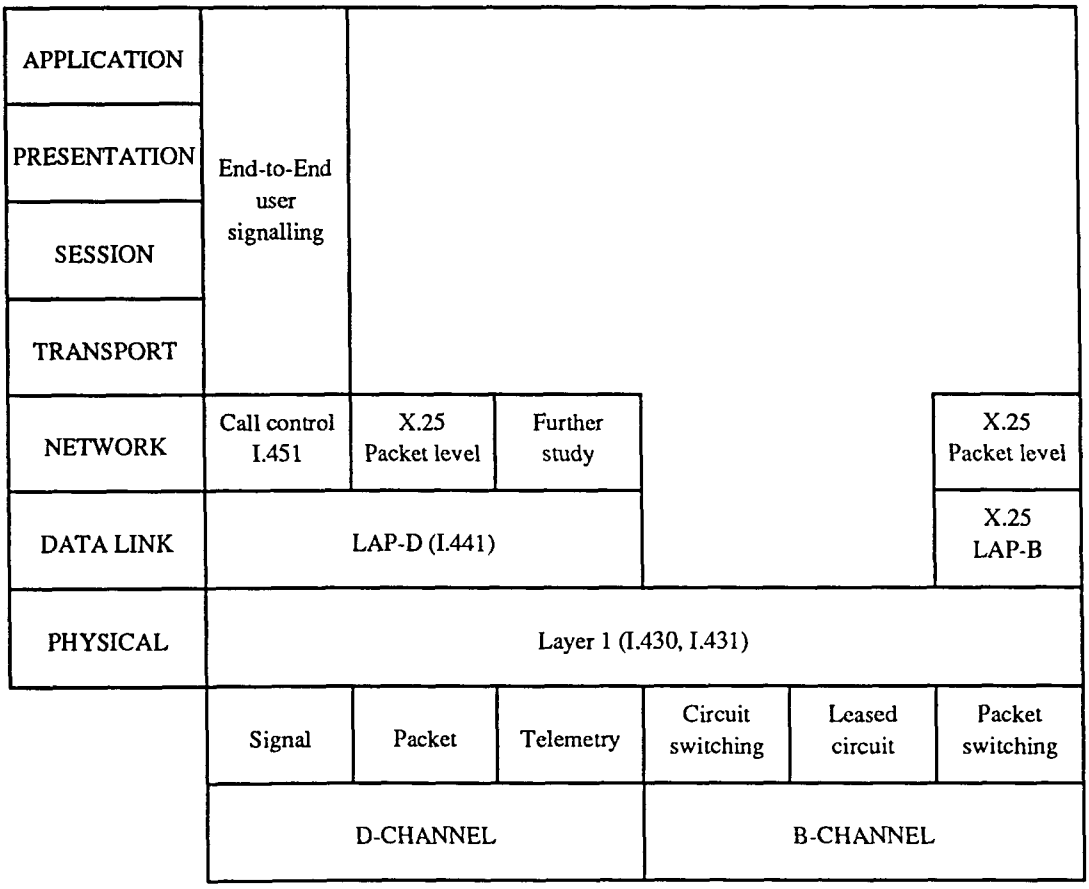


Figure 2.3: ISO/OSI model of ISDN

layer protocol is the same for both the channels. However, for layers 2-3, separate protocols are defined for the two channels. A brief description is provided for the various protocols.

The layer 1 protocol, defined in CCITT recommendations I.430 and I.431 specifies the physical interface for both, basic and primary access. The physical layer may be accessed by the user at the S, T, or U reference point. The following functions are included for this layer:

1. Encoding of digital data for transmission across the interface

2. Full duplex transmission of B-channel data

3. Multiplexing of channels to form basic or primary access transmission structure

4. Activation and deactivation of physical circuit

5. Power feeding from the network termination to the terminal

6. Terminal identification

7. Faulty terminal isolation

8. D-channel contention access

The layer 2 protocol, defined by LAP-D and LAP-B for D-channel and B-channel respectively, provide the following services:

1. Establishing and deestablishing connections

2. Error control

3. Flow control

4. Simple Link management

The Link Access Protocol for D-channel(LAP-D) is explained in Chapter 3.

The layer 3 protocol, defined by Q.930(general aspects) and Q.931(specifications) serves the purpose of establishing, maintaining, and clearing network connections such as:

- Circuit switched connections using the B-channel

- Packet switched connections using either B or D-channel
- User to user signalling connections using the D-channel

The functions performed by Q.931 can be summarized to be as follows:

- processing of primitives for communicating with data link layer
- generation and interpretation of layer 3 messages for peer-level communication
- administration of timers and logical entities (e.g., call-references) used in the call control procedures
- administration of access resources including B-channels and packet-layer logical channels
- checking to ensure that services provided are consistent with user requirements
- routing and relaying
- segmentation and reassembly

CHAPTER 3. ISDN CENTRAL OFFICE

As mentioned earlier chapter, three cards constitute the central office:

- S/T Interface card
- U interface card
- Switch card

A conceptual view of the central office is shown in Figure 3.1. The hardware design of the above cards can be found in the references [4], [5], and [6]. Since this thesis is based on the S/T interface card, the first section discusses the general aspects of the card. The second section focuses on the data link layer protocol (LAP-D).

S/T Interface Card

The block diagram of the card is shown in Figure 3.2. The main sections of this card are:

- Line interface (MT8930)
- Microprocessor system
- Interrupt control
- DP-RAM

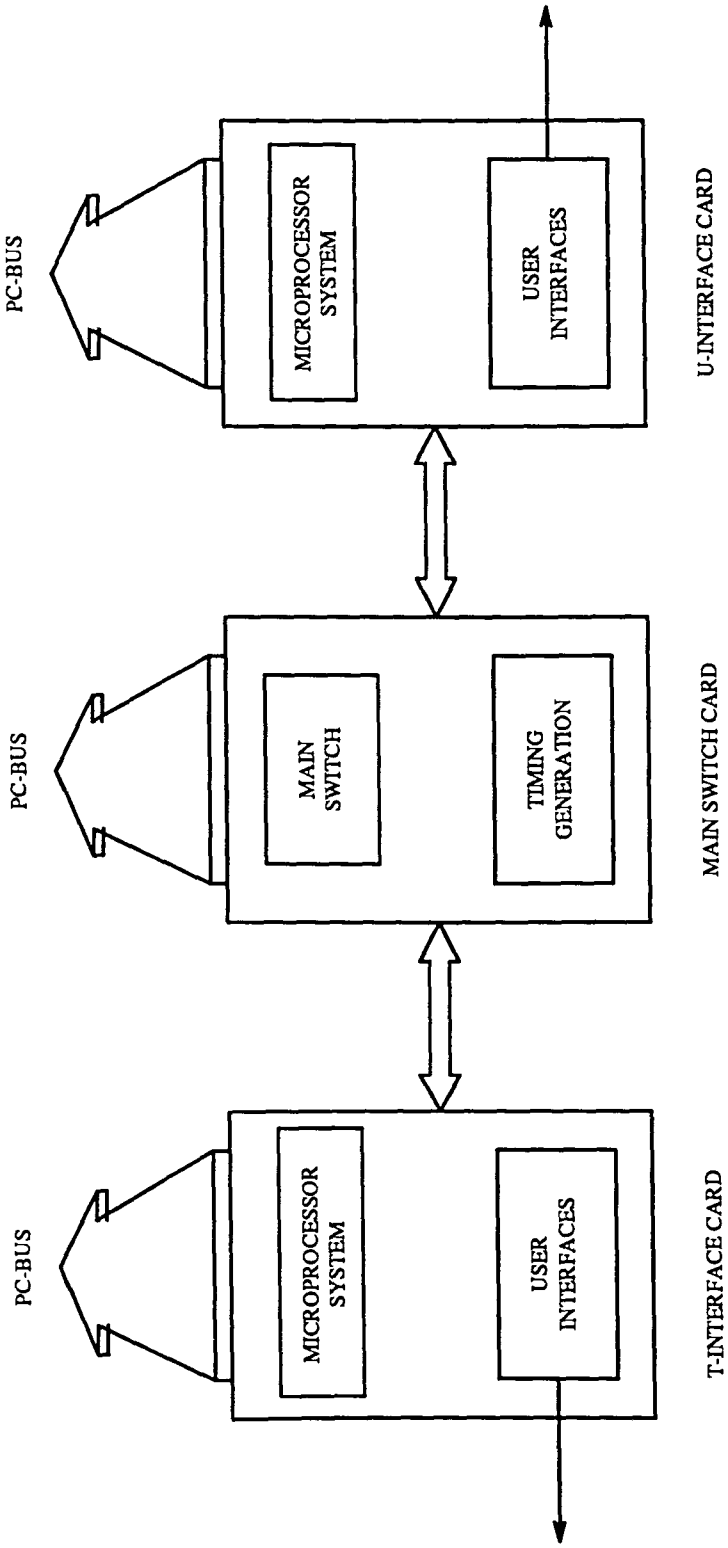


Figure 3.1: Conceptual view of the central office

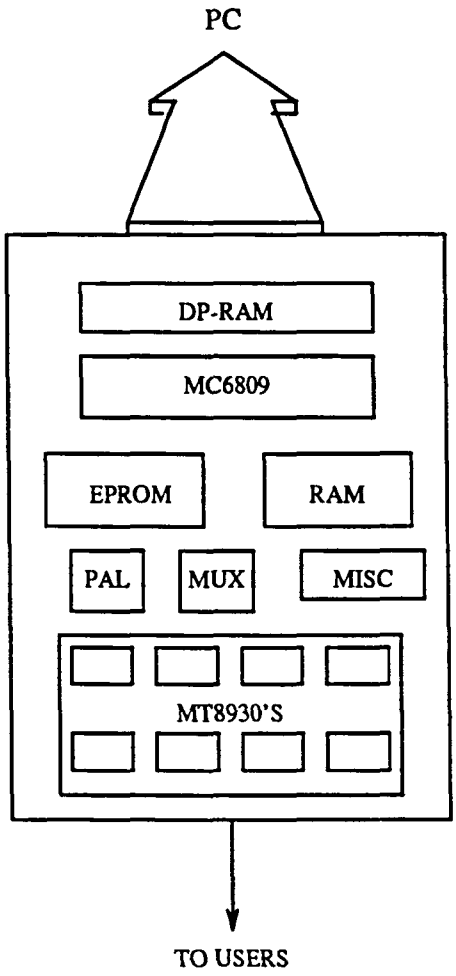


Figure 3.2: T-interface board block diagram

Line Interface

This forms the heart of the S/T interface. The chip used is the Mitel Subscriber Network Interface Circuit (SNIC) MT8930 [7]. The ISDN cable terminates on this chip through a line terminating circuit. The SNIC supports the 192 kbps (2B + D) full duplex data transmission on a 4 wire balanced transmission line. Transmission capability for both the channels is provided on the chip. The state activation mechanism built in the chip allows the customers terminals (TE's) to be

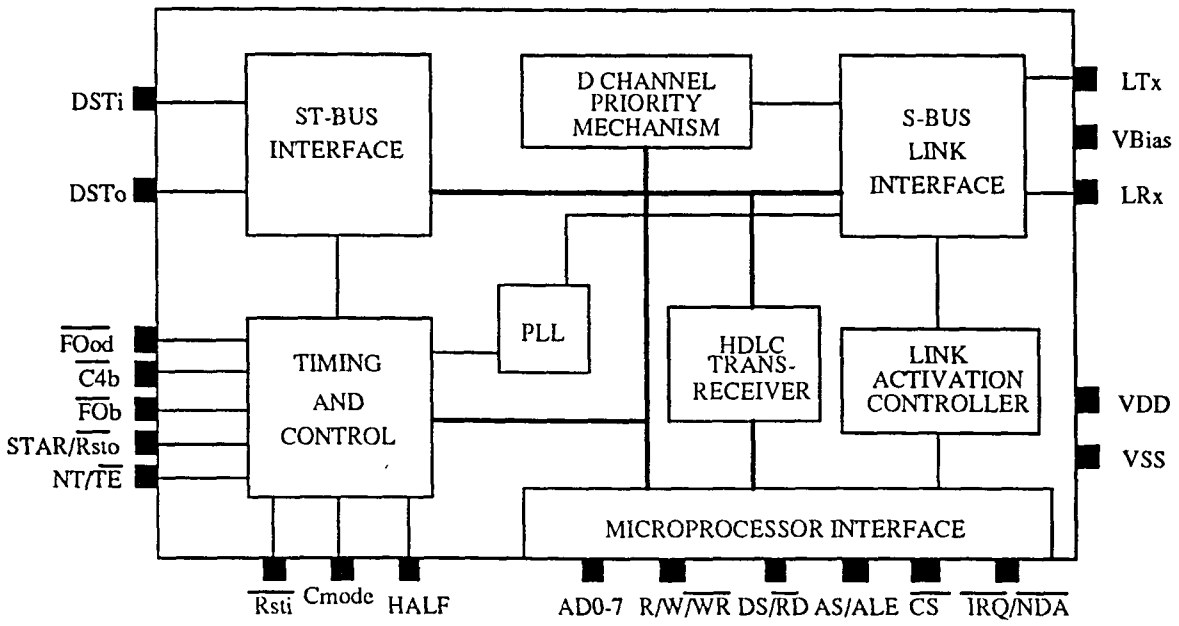


Figure 3.3: MT8930 block diagram

activated/deactivated. The SNIC also handles the resource allocation and prioritization for D-channel access contention. The control registers further allow maintenance function and monitoring of the chip.

A HDLC trans-receiver is included on the SNIC for link access protocol handling on the D-channel. Packet assembly and disassembly (PAD) functions form part of the function of the hardware. Depacketized data can be transferred between the 19 byte deep FIFO's and the microprocessor controlling the chip. Separate FIFO's exist for transmit and receive operations. The transmitter and the receiver can be separately activated/deactivated. Further, port selection is possible for either of them between a serial S-bus port and a ST-bus port. Also the transreceiver can be programmed for one or two byte address recognition. Figure 3.3 shows a block diagram of the

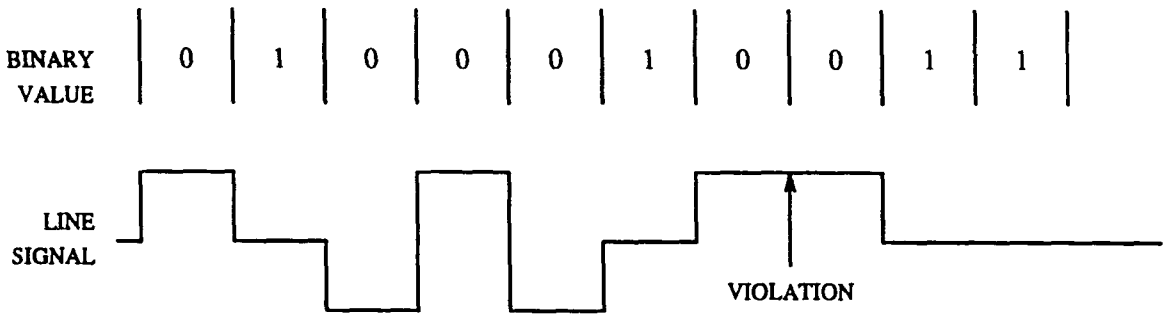


Figure 3.4: S/T interface line code

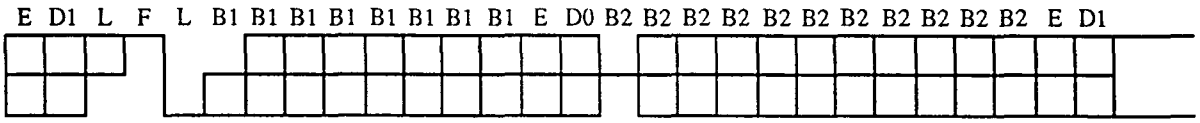
MT8930.

As can be seen from Figure 3.3, there are four major blocks of the chip:

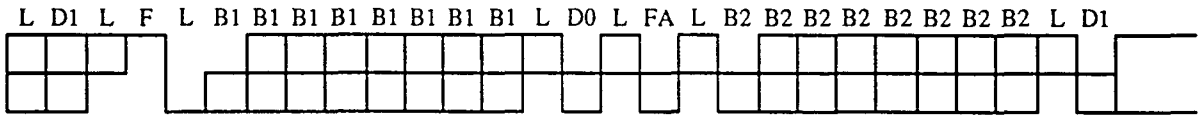
- S-Bus interface
- ST-Bus interface
- Microprocessor interface
- HDLC Transreceiver

1. **S-Bus interface:**

   (a) **Signalling standards:** This is a serial port interface provided on the chip to conform to the ISDN S/T signalling standards for Basic Rate Interface (see Figure 2.1). The line code used on the S-interface is a Psuedoternary code with 100% pulse width. Binary zeros are represented as marks on the line and the successive marks will alternate in polarity. Figure 3.4 shows an example line code.



(a) TE to NT frame structure



(b) NT to TE frame structure

Figure 3.5: Frame structures

The frame structure of the signal on this interface varies upon whether the transmission is from the NT to the TE or from the TE to the NT. A typical frame consists of the following bits (refer Figure 3.5):

- Framing bit(F)
- B1 and B2 channels(B1,B2)
- DC balancing bits(L)
- D-channel bits(D0,D1)
- Auxiliary framing and N bit(Fa,N)
- Activation bit(A)
- D-channel echo bits(E)
- Multiframing bit(M)
- Spare bit(S)

The F bit is used to mark the boundaries of a frame. The DC balancing bits are set to a negative pulse to balance the voltage. Thus, these bits occur after B1, B2, and D channel bits. The Fa and N bits are used in multiframe structures. The D-channel echo bit is a retransmission by the NT of the most recently received D bit from the TE. The A bit is used to activate/deactivate the S-Bus. The M bit is used in multiframing and the S bit is reserved for future standardization.

(b) **S-Bus activation:** The SNIC activates or deactivates the S-Bus in response to line activity or external command. The activation/deactivation controller is completely hardware driven and need not be initialized by the microprocessor. Figure 3.6 shows the state diagram for initialization. The activation protocol for an NT works as follows:

i. In the deactivated state, the NT does not assert any signal(Info0).

ii. If the NT detects Info1, it begins to transmit Info2 which consists of an S-Bus frame with zeros in the B and D-channel and activation bit(A-bit) set to zero.

iii. Once the TE synchronizes with Info2 and responds with a valid S-Bus frame with data in the B1, B2, and D-channel(Info3), the NT responds with a valid S-Bus frame.

(c) **D-channel priority mechanism:** As explained in Chapter 2, in a point-to-multipoint configuration, contention arises between the various TE's for accessing the D-channel. Allocation of the D-channel is accomplished by monitoring the E bit. Typically a TE requesting the D-channel transmits a D bit and monitors the E bit. If there is contention for the D-channel,

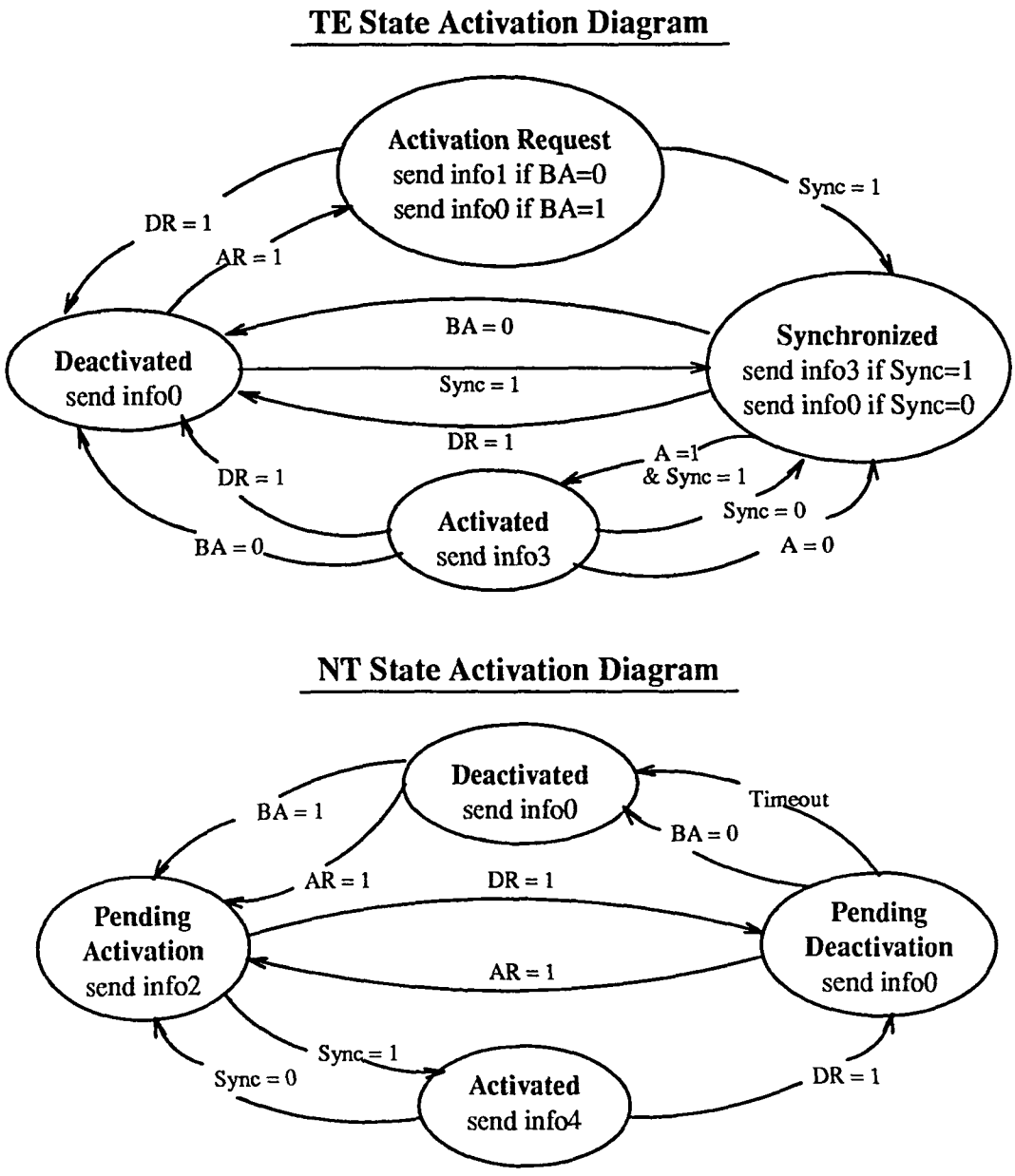


Figure 3.6: Link activation protocol, state diagram

the transmitted D bit suffers collision and the E bit will differ from the transmitted D bit. The TE then stops transmitting and waits for a specific time before requesting the channel again. If however, the E bit is the same as the transmitted D bit, then the TE gains access to the D-channel and starts transmitting. This contention is prioritized such that signalling information has priority over all other types of information. To arbitrate TE's in the same class of priority, the following mechanism is adopted [3]:

- A TE is given a low priority level within its class after successfully transmitting a layer 2 frame.
- The TE is returned to its normal level of priority within a priority class when all the TE's within the priority class have had an opportunity to transmit information.

The above mechanism is based on the requirement that a TE may start layer 2 frame transmission only when C, the current value of count is greater than or equal to the value of X1 for priority class 1 or X2 for priority class 2 (see Figure 3.7). For signalling information on the D-channel, X1=8 for normal priority level and X1=9 for lower level. For packetized data access to the D-channel, X2=10 for normal priority level and X2=11 for lower level. When a Te has successfully transmits a layer 2 frame, the value of X1 or X2 changes from a normal priority level to a lower level. After all other TE's have an opportunity to transmit, the value of X1 or X2 changes back to the normal priority level.

(d) **Wiring configuration:** Three different wiring configurations are possible based on the ISDN standards for the S/T interface:

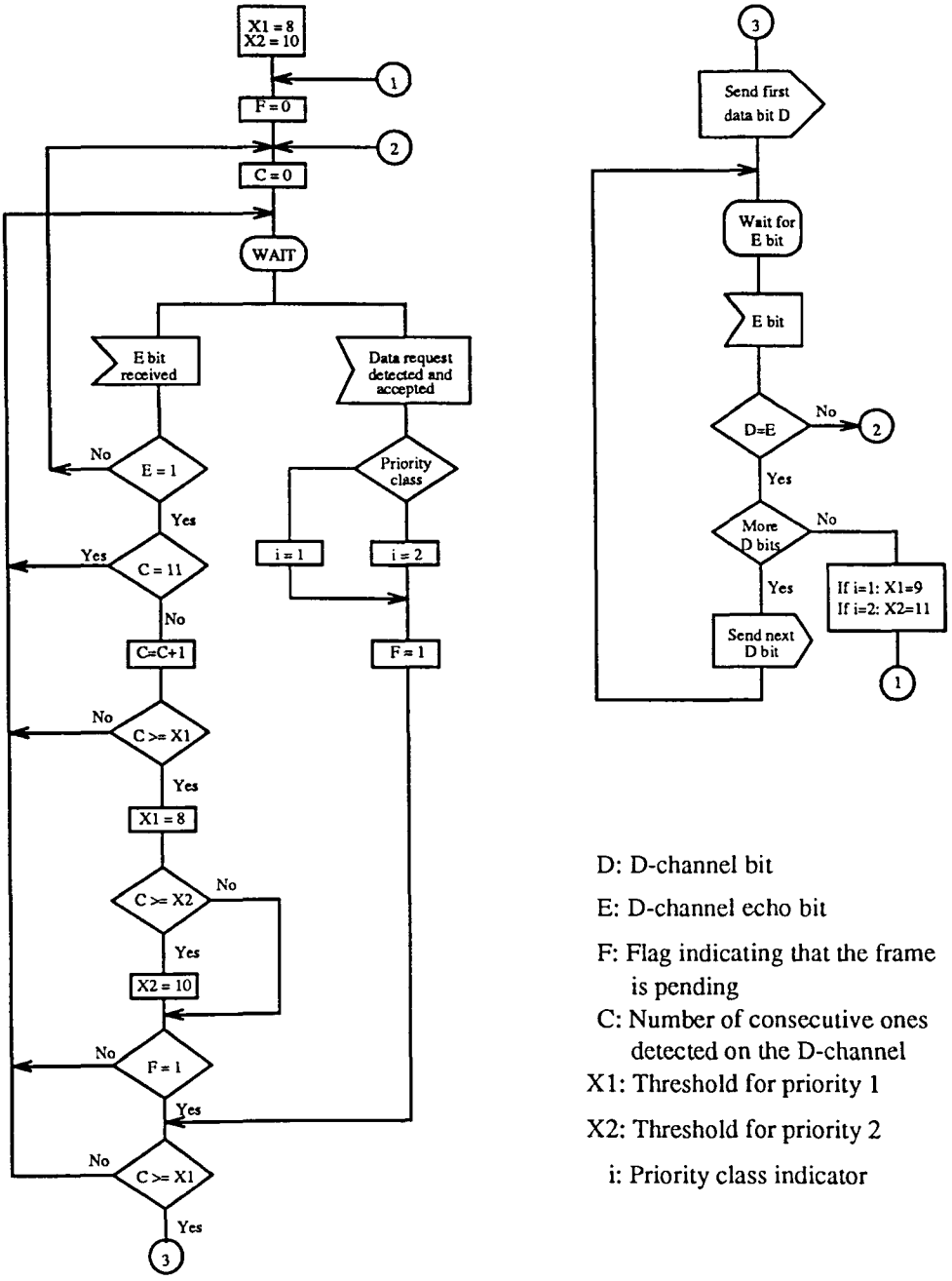


Figure 3.7: D-channel contention algorithm

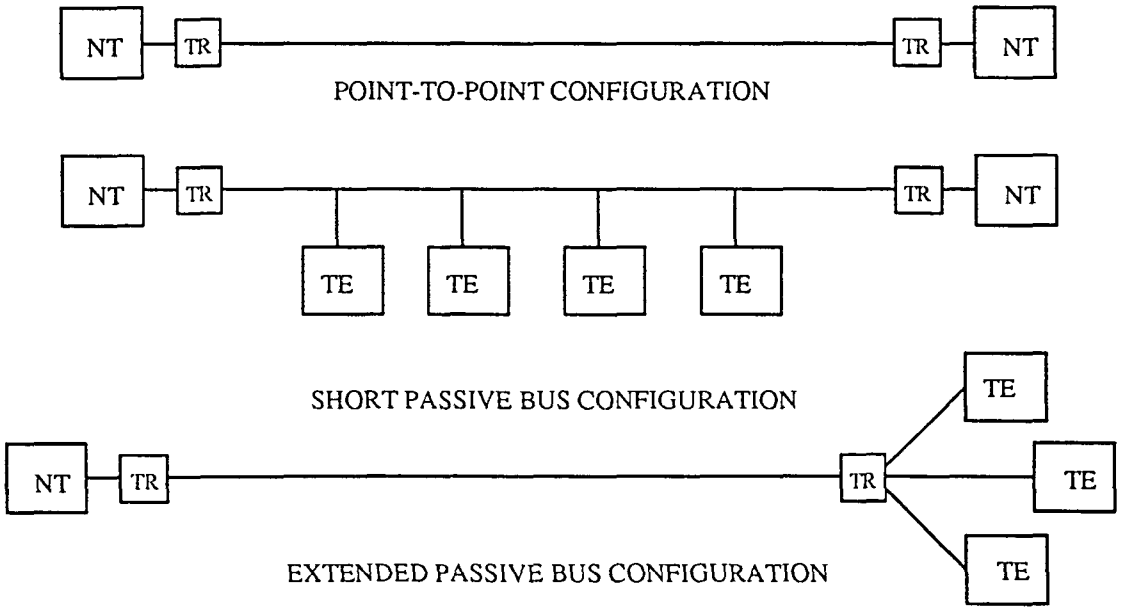


Figure 3.8: S/T interface wiring options

i. Point to Point

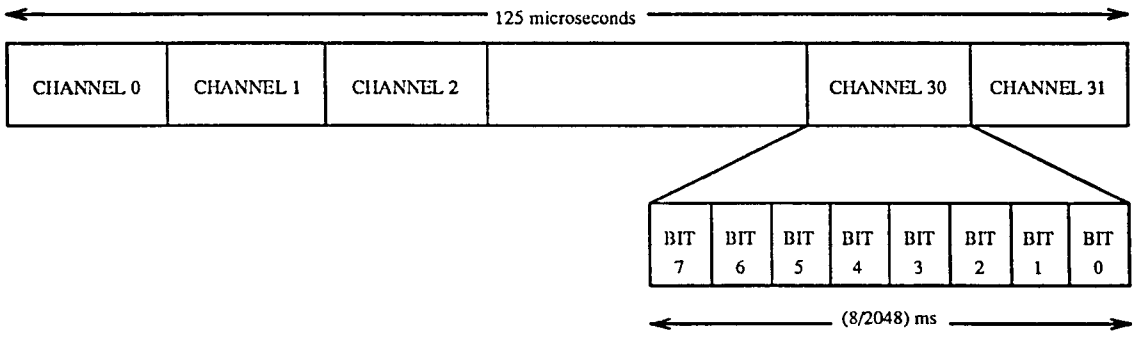
ii. Short Passive Bus

iii. Extended Passive Bus

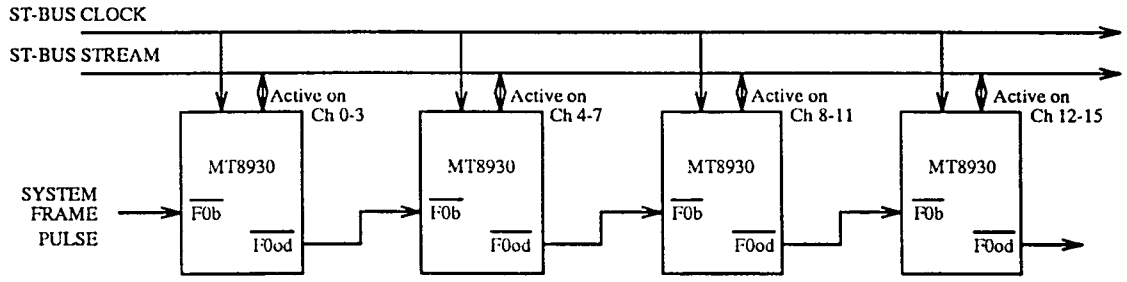
The MT8930 is chosen to operate in the Short Passive Bus configuration which is shown in Figure 3.8. For testing however, the point to point mode was used.

2. **ST-Bus interface:**

The ST-Bus is a synchronous time division multiplexed serial bus with data rate capability of 2048 kbit/s configured as 32, 64 kbit/s channels (see Figure 3.9). This conforms to the ISDN S/T interface transmission standards. In the S/T interface card, this bus is used for communication with the switch card and



(a) ST-BUS structure



(b) MT8930 daisy-chaining configuration

Figure 3.9: MT8930 ST-Bus channel configuration

the U-interface card. The eight MT8930's in the S/T card are daisy chained and occupy the entire ST-Bus stream. Serially, each MT8930 occupies the 4 channels i.e., first MT8930 occupies channels 1-4, second MT8930 occupies channels 5-8 and so on till the last MT8930 occupies channels 28-31.

3. **Microprocessor interface:**

The parallel port on the SNIC can be used as a general purpose microprocessor interface or as a hardwired control port. Consequently, the SNIC can be operated either in the microprocessor control mode (Cmode=1) or in the controllerless mode (Cmode=0).

Table 3.1: SNIC address map

	Address Lines					Write	Read
	A4	A3	A2	A1	A0		
	0	0	0	0	0	Master Control Register	verify
	0	0	0	0	1	ST-BUS Control Register	verify
A	0	0	0	1	0	HDLC Control Register	verify
S	0	0	0	1	1	HDLC Control Register 2	HDLC Status Register
Y	0	0	1	0	0	HDLC Interrupt Mask Register	HDLC Interrupt Status Register
N	0	0	1	0	1	HDLC TxFIFO	HDLC RxFIFO
C	0	0	1	1	0	HDLC Address Byte #1 Register	verify
	0	0	1	1	1	HDLC Address Byte #2 Register	verify
	0	1	0	0	0	C-channel Register	DSTi C-channel
	0	1	0	0	1	DSTo C-channel	C-channel Status Register
S	0	1	0	1	0	S-Bus Tx D-channel	DSTi D-channel
Y	0	1	0	1	1	DSTo D-channel	S-Bus RxD-channel
N	0	1	1	0	0	S-Bus TxB1-channel	DSTi B1-channel
C	0	1	1	0	1	DSTo B1-channel	S-Bus RxB1-channel
	0	1	1	1	0	S-Bus TxB2-channel	DSTi B2-channel
	0	1	1	1	1	DSTo B2-channel	S-Bus RxB2-channel

In the S/T card, the SNIC is operated in the controllerless mode. In this mode, the microprocessor has direct control over the control/status registers of the SNIC.

The first eight registers (Asynchronous registers) can be accessed at any instance. The next eight registers (Synchronous registers) however, can be accessed only when the New Data Available signal is low (refer Figure 3.3). Any read or write to these registers during a high results in erroneous data in the respective register. Table 3.1 lists the various registers with their descriptions.

4. **HDLC transreceiver:**

The HDLC transreceiver handles the bit oriented protocol structure and formats the D-channel data in accordance with the ISDN layer 2 protocol(LAP-D). A detailed discussion on this protocol is provided in the later sections. A typical transmit and receive operation by the transreceiver is performed as detailed below.

- **Transmit operation:** The HDLC registers are used to transmit packets over the channel. To physically transmit a packet, the transmitter is enabled by setting a bit in the HDLC control register 1. Data is written to the 19 byte deep transmit FIFO in a bytewide manner. The transmitter on detecting data in the FIFO starts transmitting an opening flag followed by the data in a serial fashion. To indicate that a particular byte is the last byte in the packet, the EOP bit in the HDLC control register 2 has to be set prior to writing the byte to the transmit FIFO. The transreceiver then calculates the frame checksum and transmits it followed by the ending flag. Care should be taken while writing data to the transmit FIFO. If data is written to a full FIFO, the new data overwrites the existing data. The status of the FIFO is recorded in the HDLC status register.
- **Receive operation:** To enable data reception, the receiver is enabled by setting a bit in the HDLC control register 1. When a flag is detected, the receiver synchronizes itself to the incoming data stream in a bytewide manner. The incoming packet is examined on a bit by bit basis. Inserted bits are removed and the frame checksum is calculated. Data bytes are then written to the 19 byte receive FIFO in a bytewide manner. In the

eventuality that the FCS is bad the data never enters the receive FIFO. All the bits written to the FIFO are flagged by two bits and can be read from the HDLC status register.

Microprocessor System

The microprocessor system on the S/T board consists of a Motorola 6809 processor, a Hitachi 6264 8K x 8 bit static RAM, an Intel 87C512 Erasable Programmable Read Only Memory (EPROM), and an Integrated Device Technology, Inc., IDT 7130SA/LA 1K x 8 bit Dual-Port RAM (DP-RAM). The MC6809 uses the memory mapped addressing scheme to address the following chips:

- RAM
- EPROM
- Interrupt Controller
- Multiplexer (for the eight MT8930's)
- DP-RAM

The memory map is shown in Figure 3.10.

Interrupt Controller

When a LAP-D event occurs, interrupts are generated by the MT8930's. Since eight such devices are used, there should be way of arbitrating the interrupts from these devices. The Intel 8259A provides a way of controlling these interrupts. The interrupt controller is operated in the following modes [8]:

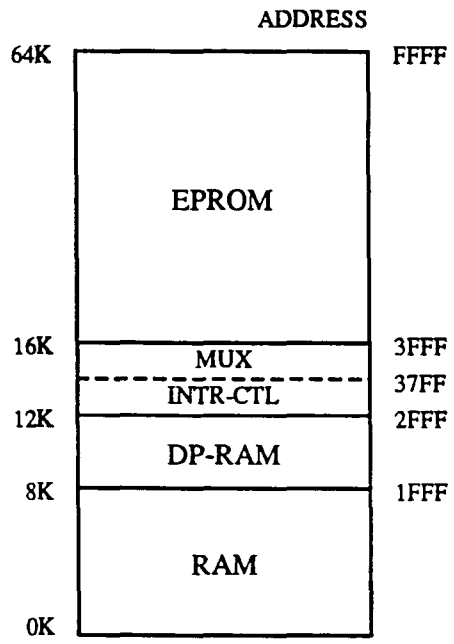


Figure 3.10: Memory map scheme

- Single, with no Master/Slave configuration
- Non-vectored operation
- Specific EOI control by the microprocessor

The above modes are selected by writing command words during initialization.

Dual-Port RAM

The Dual-Port RAM allows shared access to two ports [9]. Each port has separate control, address, and I/O pins which permits independent asynchronous access for reads and writes to the memory. Bus arbitration is built in the hardware for contention ensuing due to simultaneous write operation to a specific memory location from both the ports.

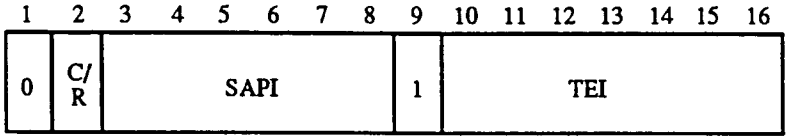
In the mailbox option an interrupt flag exists such that if data is written to a specific location($FF) by the left port, an interrupt is generated on the right port and correspondingly if data is written to a specific location($FE) by the right port, an interrupt is generated on the left port. The MC6809 on the S/T card and the IBM-PC communicate using this feature.

HDLC/LAP-D

LAP-D (Link Access Protocol for D-channel) is used for packet transmission / reception over an ISDN physical layer. Figure 3.11 shows a standard LAP-D frame.

- Flag: 01111110
- Address:
    1. EA: Address field extension bit
    2. C/R: Command/Response field bit
    3. SAPI: Service Access Point Identifier
    4. TEI: Terminal Endpoint Identifier
- Control:
    1. Information Frame (I-frame)
    2. Supervisory Frame (S-frame)
    3. Unnumbered Frame (U-frame)
- Information

(a) Frame format

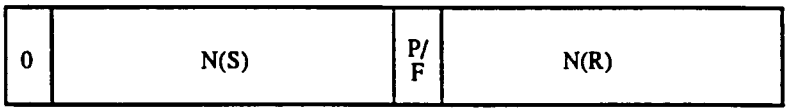


C/R = Command / rsponse

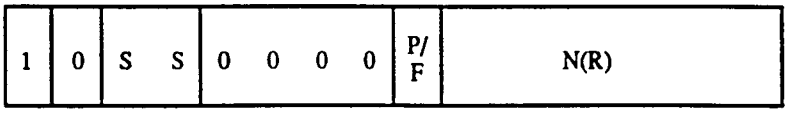
SAPI = Service access point identifier

TEI = Terminal endpoint identifier

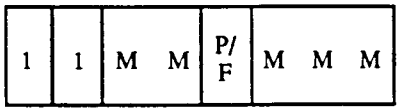
(b) Address field format



Information transfer



Supervisory



Unnumbered

N(S) = Transmitter send sequence number

N(R) = Transmitter receive sequence number

S = Supervisory function bit

M = Modifier function bit

P / F = Poll / Final bit

(c) Control field formats

Figure 3.11: Standard LAP-D frame

- FCS: Frame Check Sequence

Flag: This delimits the endpoints of a packet. A single flag may be used as the closing flag of one frame and the starting flag of the next. In order that a frame with the bit sequence the same as the flag is not misinterpreted, bit stuffing is employed. The transmitter inserts a 0 bit after all sequences of five contiguous 1 bits to ensure transparency. The receiver on the other hand, examines the data between the opening and closing flags and discards any 0 bit that directly follows a sequence of five contiguous 1 bits.

Address: Unlike standard HDLC frames, the address field of a LAP-D frame is made of two parts - Service Endpoint Identifier (SAPI) and Terminal Endpoint Identifier (TEI). This is because the LAP-D frame has to deal with two levels of multiplexing:

1. at the subscriber site where multiple user devices may share a common physical interface

2. within each user device where multiple types of traffic (e.g., data, voice, signalling) may be transmitted simultaneously (SAPI).

C/R: Lap-D packets are categorized as commands or responses. The C/R bit provides information on this aspect.

Control:

- I frames carry the data to be transmitted. Error and flow control data using the go-back-NARQ mechanism are also piggybacked on these I frames.

- S frames are used to acknowledge the reception of packets when no data is to be sent i.e. when there is no piggybacking.

- U frames are used to support unacknowledged operation and some amount of link control.

Information: This field is present only for I-frames and some U-frames. The maximum length of this field is 260 octets.

FCS: This is an error detecting code for all the bits of the frame excluding the flags. The CRC code is used in calculating FCS. As mentioned above, LAP-D may be implemented as an acknowledged or unacknowledged operation. In this research, the acknowledged mode is employed. This involves the exchange of I, S, and U frames. Table 3.2 lists the various commands and responses for an acknowledged operation.

Table 3.2: LAP-D commands and responses

Name	*Control Field Encoding*	*C/R*	*Description*
	Information Transfer Format		
I (Information)	0-N(S)--P-N(R)--	C	Exchange user data
	Supervisory Format		
RR (Receive Ready)	10000000*-N(R)--	C/R	Positive ack; ready to receive frame
RNR (Receive Not Ready)	10100000*-N(R)--	C/R	Positive ack; not ready to receive
REJ (Reject)	10010000*-N(R)--	C/R	Negative ack; go back N
	Unnumbered Format		
SABME (Set Asynchronous Balanced Mode)	1111P110	C	Request logical connection
DM (Disconnected Mode)	1111F000	R	Unable to establish or maintain logical connection
UI (Unnumbered Information)	1100P000	C	Used for unacknowledged information transfer service
DISC (Disconnect)	1100P010	C	Terminate logical connection
UA (Unnumbered Acknowledgment)	1100F110	R	Acknowledge SABME or DISC
FRMR (Frame Reject)	1110F001	R	Reports receipt of unacceptable frame
XID (Exchange Identification)	1111*101	C/R	Exchange identification information

* = P/F bit

CHAPTER 4. IMPLEMENTATION OF LAP-D FOR S/T INTERFACE

Since the implementation involves the IBM-PC and the S/T interface card this chapter is divided into 2 sections:

- S/T Interface section
- PC section

S/T Interface

This section is written entirely in MC 6809 assembly language. As mentioned earlier, the S/T card communicates with the PC through the DP-RAM (address 2000H - 23FFH). The software is entirely interrupt driven. Before explaining the actual implementation details, the listing of the assumptions is in order:

1. The terminal endpoint identifier (TEI) of the central office is 10.
2. The service access point identifier (SAPI) is chosen as 16.
3. Data transfer is through the B channel with only the connection setup over the D channel.

A conceptual design of the software is shown in Figure 4.1.

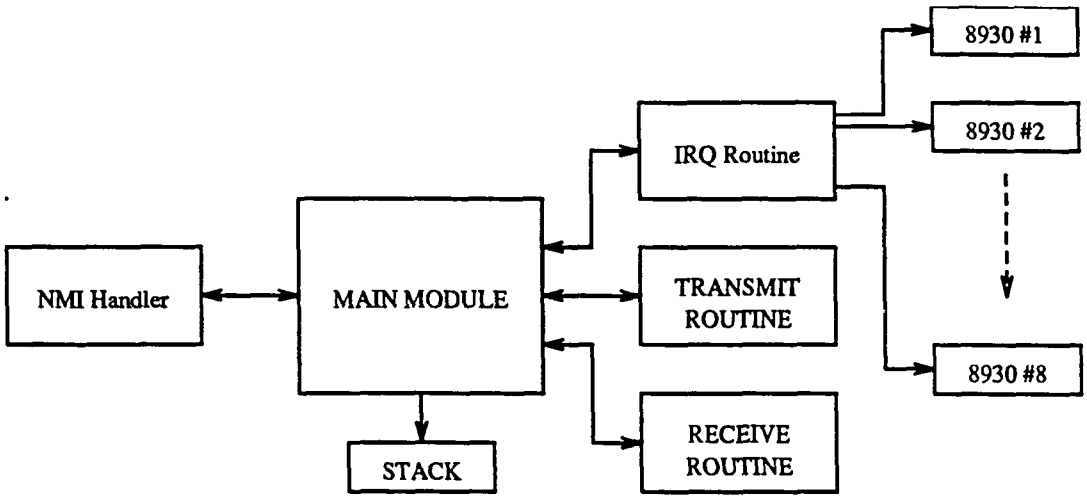


Figure 4.1: Conceptual software design

- *Main module*: In this module all the interface chips are initialized. The initialization parameters are as follows:

  - *Interrupt controller*:

    OCW1 : 00010010

    ICW2 : 00000000

    OCW1 : 11111111

    OCW2 : 01100000

  - *SNIC*:

    Master Control Register: 00000111

    ST-Bus Control Register: 11111111

    HDLC Control Register 1: 01011101

    HDLC Control Register 2: 00001100

    HDLC Interrupt Mask Register: 11111111

    NT Mode C-channel Control Register: 10010000

Further, packet decoding is performed in this routine to ascertain the validity of packets and flow control using the go-back-N ARQ mechanism.

- *Transmit routine*: This routine handles the transmission of packets over the D channel. A software flow diagram for the formation of a packet is shown in Figure 4.2. The data space used by this routine is $2000 - $2100.

- *Receive routine*: This routine handles the reception of packets over the D channel. A software flow diagram of the reception of a packet is shown in Figure 4.3. The data space used by this routine is $2100 - $2200.

- *IRQ Service Routine*: Since the 8259 is not used in the vectored mode, the actual interrupt line being serviced has to be identified. In this routine, the respective registers of 8259 are read and the interrupt identified.

- *NMI Handler*: This is a PC driven interrupt (IRQ 4). In this routine, the buffer in the DP-RAM ($2300 - $2320) is read for necessary action to be taken by the S/T card. For e.g, a call setup request by the PC causes an NMI interrupt. The data in the above mentioned buffer specifies the TEI, SAPI, and control information of the destination TE.

PC section

In the original design of the central office, the PC was was supposed to handle the layer 3 software (Q.931). This is part of the future enhancement to the central office. The only software existing on the PC at present is the interrupt service routine for IRQ4. This forms the base of the layer 2 software for the S/T interface.

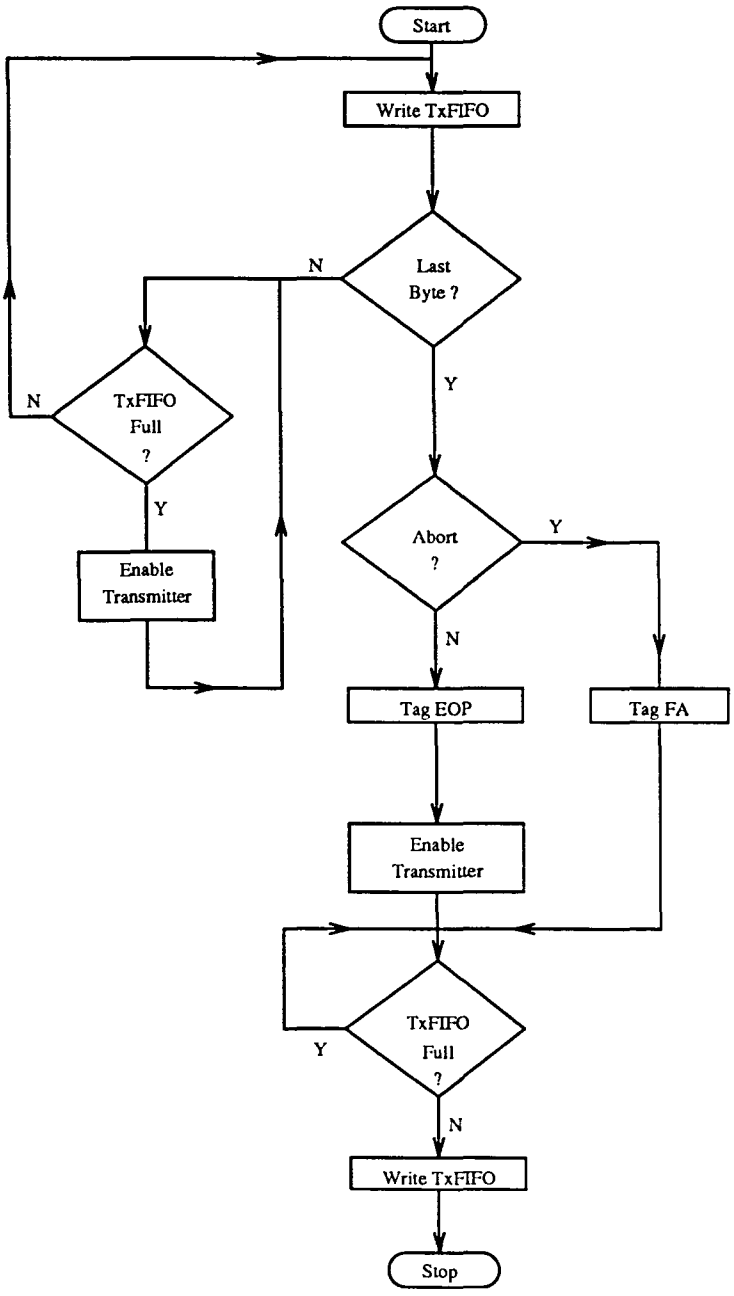


Figure 4.2: Transmit packet algorithm

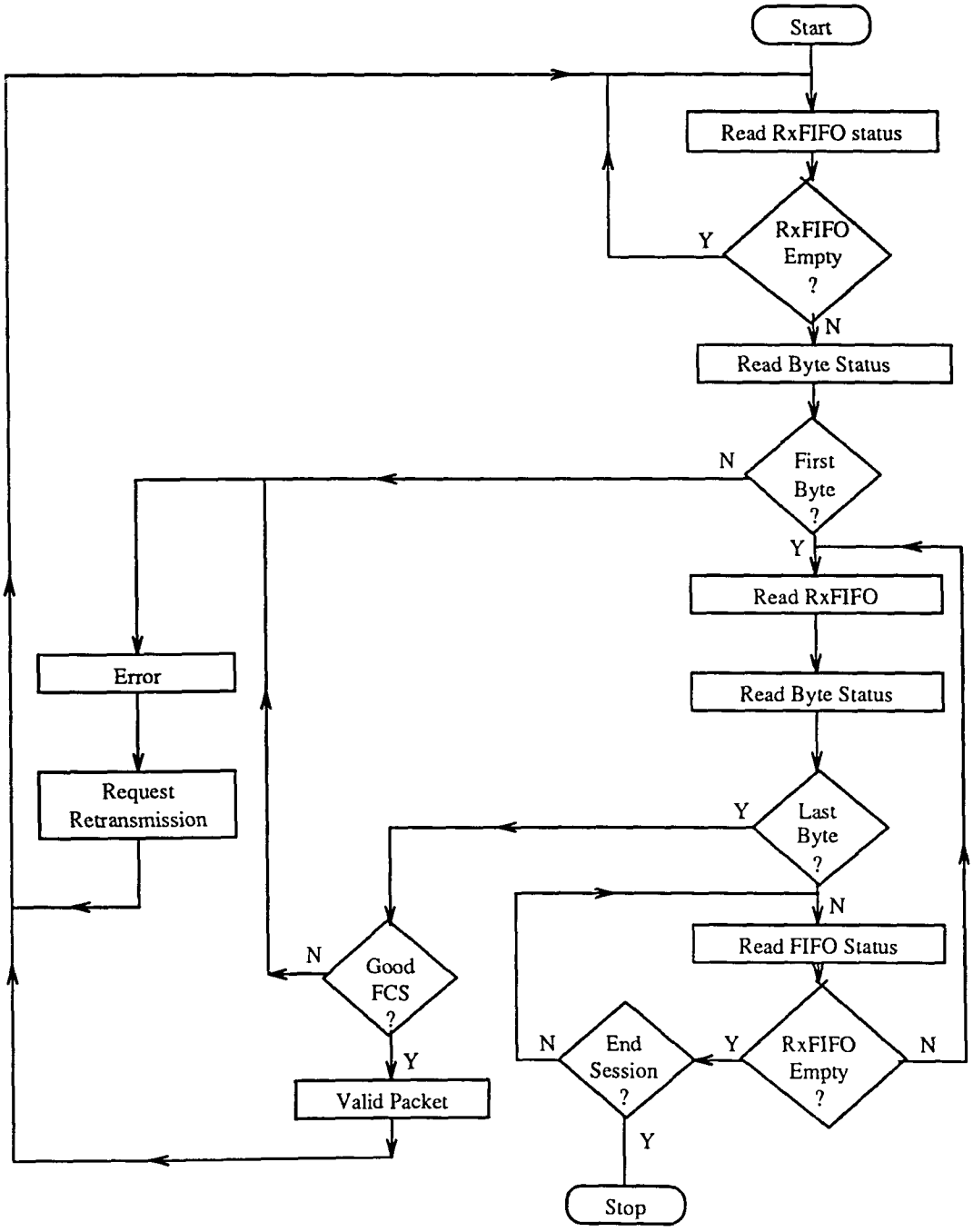


Figure 4.3: Receive packet algorithm

There are two parts to this routine:

- Terminate and Stay Resident (TSR) program
- Interrupt handler

The TSR is written entirely in 80x86 assembly language. There are two parts to this routine. The first part involves the modification of the PC interrupt vector table while the second part involves the restoration of the same. BIOS interrupts were used in the implementation. The small memory model used for the compilation.

The Interrupt handler deals with the decoding of the LAP-D packets. The routine reads the data from the DP-RAM and performs the necessary upper layer operations. At present, however, it reads the data from the DP-RAM and requests the S/T card to transmit an acknowledgment packet.

Based on the two sections, a typical call setup scenario over the D channel can be visualized to involve the following operations:

- A TE1 requests a call setup with the central office
- The MT8930 connecting the TE1 generates an interrupt
- The above causes an IRQ to the MC6809 upon which the IRQ routine is activated. In this process the interrupting MT8930 is recognized.
- The receive routine then gets activated and the data is read from the receive FIFO and written to the DP-RAM.
- The above operation generates an interrupt to the PC which causes the PC interrupt handler routine to be activated. Data is then decoded and a reply packet data is written back to the DP-RAM.

- This causes the S/T card to be interrupted again. The NMI handler is activated and the data from the DP-RAM is packetized.
- The transmit routine is then executed and the packet is written to the TxFIFO for eventual transmission.

Software consideration

The New Data Available signal indicating newly arrived packets has a periodicity of 125 usec. This imposes a restriction on the execution time of the interrupt service routine on the S/T card. If the interrupt routine has an execution time more than 125 usec, then there is a chance of missing an interrupt. The shorter the execution time, the better is the performance.

CHAPTER 5. CONCLUSION

The realization of this project is a working central office for the laboratory environment. Currently, it allows upto 64 S/T-interface devices and 8 U-interface devices to communicate through the Basic Rate Interface technology. The switch card has been designed to have sufficient capacity to switch 256 inputs and outputs using the MITEL ST-Bus. In order to handle the transmission speed of the S/T and U interfaces, a MC6809 processor is used on both the cards. The IBM-compatible Personal Computer handles the higher level software and monitoring operations.

After wiring the line interface circuit for the MT8930, I performed basic hardware interface tests for the chips. I wrote a monitor program for testing the various chips on board and the communication between the PC and the S/T card through the DP-RAM. I also wrote the layer 2 software for the card. However, no higher level operation was possible since the layer 3 software was not yet implemented. Testing was done using the Motorola MC 145490/91 EVK ISDN Evaluation Board containing the Q.921 and Q.931 software. The ISDN Evaluation Board was operated in the TE mode while the S/T card operated in the NT mode. Packets were successfully exchanged between the two stations.

Interaction between the S/T and U interface cards has not yet been tested. It

is hoped that eventually Q.931 will be implemented along with the capability for Primary Rate Interface.

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APPENDIX A. MT8930 REGISTER DEFINITIONS

Table A.1: Master control register - read/write address 00000b

BIT	NAME	DESCRIPTION
B7-B3	NA	KEEP AT '0' FOR NORMAL OPERATION.
B2	NDA/IRQ	THE STATE OF THIS PIN WILL SELECT THE MODE OF THE IRQ/NDA PIN. A '0' WILL ENABLE THE IRQ PIN FOR HDLC INTERRUPTS. A '1' WILL ENABLE THE NEW DATA AVAILABLE SIGNAL WHICH IDENTIFIES THE ACCESS TIME TO THE SYNCHRONOUS REGISTERS. (IF NDA IS ENABLED, THE HDLC INTERRUPTS ARE DISABLED).
B1	M/SEN	A '0' WILL ENABLE THE TRANSMISSION OF THE M OR S BIT AS SELECTED IN THE NT MODE C-CHANNEL REGISTER. THE SELECTION OF M OR S IS DETERMINED BY THE HALF SIGNAL. A '1' WILL DISABLE THIS FEATURE FORCING THE M AND S BITS TO BINARY ZERO.
B0	P/SC	THE PARALLEL/SERIAL CONTROL BIT SELECTS THE SOURCE OF THE CONTROL CHANNEL. IF '0', THEN THE C-CHANNEL REGISTER IS ACCESSED THROUGH THE MICROPROCESSOR PORT.

Table A.2: ST-BUS control register - read/write address 00001b

BIT	NAME	DESCRIPTION
B7	CH3i	IF '1', THEN THE INPUT ST-BUS CHANNEL 3 IS ENABLED. IF '0', THEN THE CHANNEL IS DISABLED AND WILL READ FF.
B6	CH2i	IF '1', THEN THE INPUT ST-BUS CHANNEL 2 IS ENABLED. IF '0', THEN THE CHANNEL IS DISABLED AND WILL READ FF.
B5	CH1i	IF '1', THEN THE INPUT ST-BUS CHANNEL 1 IS ENABLED. IF '0', THEN THE CHANNEL IS DISABLED AND WILL READ 00.
B4	CH0i	IF '1', THEN THE INPUT ST-BUS CHANNEL 0 IS ENABLED. IF '0', THEN THE CHANNEL IS DISABLED AND WILL READ FF.
B3	CH3o	IF '1', THEN THE OUTPUT ST-BUS CHANNEL 3 IS ENABLED. IF '0', THEN THE CHANNEL IS DISABLED AND IT WILL BE PLACED IN HIGH IMPEDANCE.
B2	CH2o	IF '1', THEN THE OUTPUT ST-BUS CHANNEL 2 IS ENABLED. IF '0', THEN THE CHANNEL IS DISABLED AND IT WILL BE PLACED IN HIGH IMPEDANCE.
B1	CH1o	IF '1', THEN THE OUTPUT ST-BUS CHANNEL 1 IS ENABLED. IF '0', THEN THE CHANNEL IS DISABLED AND IT WILL BE PLACED IN HIGH IMPEDANCE.
B0	CH0o	IF '1', THEN THE OUTPUT ST-BUS CHANNEL 0 IS ENABLED. IF '0', THEN THE CHANNEL IS DISABLED AND IT WILL BE PLACED IN HIGH IMPEDANCE.

Table A.3: HDLC control register 1 - read/write address 00010b

BIT	NAME	DESCRIPTION
B7	TxEn	A '1' ENABLES THE HDLC TRANSMITTER FOR THE SELECTED D-CHANNEL (i.e. ST-BUS OR S-BUS). A '0' DISABLES THE HDLC TRANSMITTER (i.e. AN ALL 1'S SIGNAL WILL BE SENT).
B6	RxEn	A '1' ENABLES THE HDLC RECEIVER FOR THE SELECTED D-CHANNEL (i.e. ST-BUS OR S-BUS). A '0' DISABLES THE HDLC RECEIVER (i.e. AN ALL 1'S SIGNAL WILL BE RECEIVED).
B5	ADRec	IF '1', THEN THE ADDRESS RECOGNITION IS ENABLED. THIS FORCES THE RECEIVER TO RECOGNIZE ONLY THOSE PACKETS HAVING THE UNIQUE ADDRESS AS PROGRAMMED IN THE RECEIVE ADDRESS REGISTERS OR IF THE ADDRESS BYTE IS THE ALL-CALL ADDRESS (ALL 1s). IF '0', THEN THE ADDRESS RECOGNITION IS DISABLED AND EVERY VALID PACKET IS STORED IN THE RECEIVED FIFO.
B4	TxPrtSel	THIS BIT SELECTS THE PORT OF THE HDLC TRANSMITTED D-CHANNEL. IF '1' , SELECTS THE S-BUS PORT. IF '0', SELECTS THE ST-BUS PORT.
B3	RxPrtSel	THIS BIT SELECTS THE PORT OF THE HDLC RECEIVED D-CHANNEL. IF '1', SELECTS THE S-BUS PORT. IF '0', SELECTS THE ST-BUS PORT.
B2	IFTF	THIS BIT SELECTS THE INTERFRAME TIME FILL. A '1' SELECTS CONTINUOUS FLAGS. A '0' SELECTS AN ALL 1s IDLE STATE.
B1	NA	KEEP AT '0' FOR NORMAL OPERATION.
B0	HLoop	A '1' WILL ACTIVATE THE HDLC LOOPBACK WHERE THE TRANSMITTED D-CHANNEL IS LOOPED BACK TO THE RECEIVED D-CHANNEL. THE TRANSMISSION OF THE PACKET IS NOT AFFECTED. A '0' DISABLES THE LOOPBACK.

Table A.4: HDLC control register 2 - write address 00011b

BIT	NAME	DESCRIPTION
B7-B5	NA	KEEP AT '0' FOR NORMAL OPERATION.
B4	TRANS	A '1' WILL PLACE THE HDLC IN A TRANSPARENT MODE. THIS WILL PERFORM THE SERIAL TO PARALLEL OR PARALLEL TO SERIAL CONVERSION WITHOUT INSERTING OR DELETING THE OPENING AND CLOSING FLAGS, CRC BYTES, OR ZERO INSERTION. THE SOURCE OR DESTINATION OF THE DATA IS DETERMINED BY THE PORT SELECTION BITS IN THE HDLC CONTROL REGISTER 1.
B3	RxRst	A '1' WILL RESET THE RECEIVE FIFO. THIS CAUSES THE RECEIVER TO BE DISABLED UNTIL THE RECEPTION OF THE NEXT FLAG. (THE STATUS REGISTER WILL IDENTIFY THE RxFIFO AS BEING EMPTY).
B2	TxRst	A '1' WILL RESET THE TRANSMIT FIFO. THIS CAUSES THE TRANSMITTER TO CLEAR ALL DATA IN THE TxFIFO.
B1	FA	A '1' WILL TAG THE NEXT BYTE WRITTEN TO THE TRANSMIT FIFO AND CAUSE AN ABORT SEQUENCE TO BE TRANSMITTED ONCE IT REACHES THE BOTTOM OF THE FIFO.
B0	EOP	A '1' WILL TAG THE NEXT BYTE WRITTEN TO THE TRANSMIT FIFO AND CAUSE AN END OF PACKET SEQUENCE TO BE TRANSMITTED ONCE IT REACHES THE BOTTOM OF THE FIFO.

Table A.5: HDLC status register - read address 00011b

BIT	NAME	DESCRIPTION
B7-B6	RxBYTE STATUS	THESE TWO BITS INDICATE THE STATUS OF THE RECEIVED BYTE WHICH IS READY TO BE READ FROM THE RECEIVED FIFO. THE STATUS IS ENCODED AS FOLLOWS: B7 - B6 0 - 0 PACKET BYTE 0 - 1 FIRST BYTE 1 - 0 LAST BYTE (GOOD FCS) 1 - 1 LAST BYTE (BAD FCS)
B5-B4	RxFIFO STATUS	THESE TWO BITS INDICATE THE STATUS OF THE RECEIVE FIFO ENCODED AS: B5 - B4 0 - 0 RxFIFO EMPTY 0 - 1 <= 14 BYTES 1 - 0 RxFIFO OVERFLOW 1 - 1 >= 15 BYTES
B3-B2	TxFIFO STATUS	THESE TWO BITS INDICATE THE STATUS OF THE TRANSMIT FIFO AS FOLLOWS: B3 - B2 0 - 0 TxFIFO FULL 0 - 1 >= 5 BYTES 1 - 0 TxFIFO EMPTY 1 - 1 <= 4 BYTES
B1	IDLE	IF '1', AN IDLE CHANNEL STATE HAS BEEN DETECTED.
B0	INT	IF '1', AN UNMASKED ASYNCHRONOUS INTERRUPT HAS BEEN DETECTED.

Table A.6: HDLC interrupt mask register - write address 00100b

BIT	NAME	DESCRIPTION
B7	EnGA	A '1' WILL ENABLE THE GO-AHEAD INTERRUPT SIGNAL WHICH IS IDENTIFIED BY THE RECEPTION OF 01111110. A '0' WILL DISABLE IT.
B6	EnEOPD	A '1' WILL ENABLE THE RECEIVED END OF PACKET INTERRUPT. A '0' WILL DISABLE IT.
B5	EnTEOP	A '1' WILL ENABLE THE TRANSMIT END OF PACKET INTERRUPT. A '0' WILL DISABLE IT.
B4	EnFA	A '1' WILL ENABLE THE FRAME ABORT INTERRUPT. A '0' WILL DISABLE IT.
B3	EnTxFL	A '1' WILL ENABLE THE TRANSMIT FIFO LOW INTERRUPT. A '0' WILL DISABLE IT.
B2	EnTxFun	A '1' WILL ENABLE THE TRANSMIT FIFO UNDERRUN INTERRUPT. A '0' WILL DISABLE.
B1	EnRxFF	A '1' WILL ENABLE THE RECEIVE FIFO FULL INTERRUPT. A '0' WILL DISABLE IT.
B0	EnRxFov	A '1' WILL ENABLE THE RECEIVE FIFO OVERFLOW INTERRUPT. A '0' WILL DISABLE.

Table A.7: HDLC interrupt status register - read address 00100b

BIT	NAME	DESCRIPTION
B7	GA	A '1' INDICATES THAT A GO-AHEAD SEQUENCE HAS BEEN DETECTED ON THE RECEIVED HDLC D-CHANNEL.
B6	EOPD	A '1' INDICATES THAT AN END OF PACKET HAS BEEN DETECTED ONT THE HDLC RECEIVER. THIS CAN BE IN THE FORM OF A FLAG, AN ABORT SEQUENCE OR AS AN INVALID PACKET.
B5	TEOP	A '1' INDICATES THAT THE TRANSMITTER HAS FINISHED SENDING THE CLOSING FLAG OF THE LAST PACKET IN THE Tx FIFO.
B4	FA	A '1' INDICATES THAT THE RECEIVER HAS DETECTED A FRAME ABORT SEQUENCE ON THE RECEIVED DATA STREAM.
B3	TxFL	A '1' INDICATES THAT THE DEVICE HAS ONLY 4 BYTES REMAINING IN THE Tx FIFO. THIS BIT HAS SIGNIFICANCE ONLY WHEN THE Tx FIFO IS BEING DEPLETED AND NOT WHEN IT IS GETTING LOADED.
B2	TxFun	A '1' INDICATES THAT THE Tx FIFO IS EMPTY WITHOUT BEING GIVEN THE 'END OF PACKET' INDICATION. THE HDLC WILL TRANSMIT AN ABORT SEQUENCE AFTER ENCOUNTERING AN UNDERRUN CONDITION.
B1	RxFF	A '1' INDICATES THAT THE HDLC CONTROLLER HAS ACCUMULATED AT LEAST 15 BYTES IN THE Rx FIFO.
B0	RxFov	A '1' INDICATES THAT THE Rx FIFO HAS OVERFLOWN (i.e. AN ATTEMPT TO WRITE TO A FULL Rx FIFO). THE HDLC WILL ALWAYS DISABLE THE RECEIVER ONCE THE RECEIVE OVERFLOW HAS BEEN DETECTED. THE RECEIVER WILL BE RE-ENABLED UPON DETECTION OF THE NEXT FLAG.

Table A.8: HDLC address recognition register 1 - read/write address 00110b

BIT	NAME	DESCRIPTION
B7-B2	R1A7-R1A2	A SIX BIT MASK USED TO INTERROGATE THE FIRST BYTE OF THE RECEIVED ADDRESS (WHERE B7 IS MSB). IF ADDRESS RECOGNITION IS ENABLED, ANY PACKET FAILING THE ADDRESS COMPARISON WILL NOT BE STORED IN THE Rx FIFO.
B1	NA	NOT APPLICABLE TO ADDR RECOGNITION.
B0	A1En	IF '0', THE FIRST BYTE OF THE ADDRESS FIELD WILL NOT BE USED DURING ADDRESS RECOGNITION. IF '1' AND THE ADDRESS RECOGNITION IS ENABLED, THE 6 MOST SIGNIFICANT BITS OF THE FIRST ADDRESS BYTE WILL BE COMPARED WITH THE FIRST 6 BITS OF THIS REGISTER.

Table A.9: HDLC address recognition register 2 - read/write address 00111b

BIT	NAME	DESCRIPTION
B7-B1	R2A7-R2A1	A SEVEN BIT MASK USED TO INTERROGATE THE SECOND BYTE OF THE RECEIVED ADDRESS (WHERE B7 IS MSB). IF ADDRESS RECOGNITION IS ENABLED, ANY PACKET FAILING THE ADDRESS COMPARISON WILL NOT BE STORED IN THE Rx FIFO. THIS MASK IS IGNORED IF THE ADDRESS IS A BROADCAST.
B0	A2En	IF '0', THE SECOND BYTE OF THE ADDRESS FIELD WILL NOT BE USED DURING ADDRESS RECOGNITION. IF '1' AND THE ADDRESS RECOGNITION IS ENABLED, THE SEVEN MOST SIGNIFICANT BITS OF THE SECOND ADDRESS BYTE WILL BE COMPARED WITH THE FIRST SEVEN BITS OF THIS REGISTER.

Table A.10: NT mode c-channel control register - read/write 01000b and B0=0

BIT	NAME	DESCRIPTION
B7	AR	SETTING THIS BIT WILL INITIATE THE ACTIVATION OF THE S-BUS. IF '0', THE DEVICE WILL REMAIN IN THE PRESENT STATE.
B6	DR	SETTING THIS BIT WILL INITIATE THE DEACTIVATION OF THE S-BUS. IF '0', THE DEVICE WILL REMAIN IN ITS PRESENT STATE. THIS BIT HAS PRIORITY OVER AR.
B5	DinB	IF '1', THE D-CHANNEL WILL BE PLACED IN THE B1 TIME SLOT ALLOCATING 64 KBPS TO THE D-CHANNEL. IF '0', THE D-CHANNEL WILL ASSUME ITS POSITION WITH A 16 KBPS BANDWIDTH.
B4	TIMING	A '0' WILL SET THE NT IN A SHORT PASSIVE BUS CONFIGURATION USING A FIXED TIMING SOURCE (NO COMPENSATION FOR LINE LENGTH). A '1' WILL SET THE NT IN A POINT-TO-POINT OR EXTENDED PASSIVE BUS CONFIGURATION WITH ADAPTIVE TIMING COMPENSATION.
B3	M/S	THIS BIT REPRESENTS THE STATE OF THE TRANSMITTED M/S-BIT. M WHEN HALF=0 AND S WHEN HALF=1.
B2	HALF	THE STATE OF THIS BIT IDENTIFIES WHICH HALF OF THE FRAME WILL BE TRANSMITTED ON THE S-BUS.
B1	TxMFR	A '1' IN THIS BIT WILL FORCE THE TRANSMISSION OF A MULTIFRAME SEQUENCE IN THE Fa AND N BITS i.e. Fa=1 AND N=0. A '0' WILL RESUME NORMAL OPERATION i.e. Fa=0 AND N=1.
B0	RegSel	IF THE REGISTER SELECT BIT IS SET TO '1', THE CONTROL REGISTER IS REDEFINED AS THE DIAGNOSTIC REGISTER. A '0' GIVES ACCESS TO THE CONTROL REGISTER.

Table A.11: NT mode c-channel diagnostic register - write address 01000b and B0=1

BIT	NAME	DESCRIPTION
B7-B6	LOOP	THE STATUS OF THESE 2 BITS DETERMINE WHICH TYPE OF LOOPBACK IS TO BE PERFORMED: B7-B6 TYPE 0-0 NO LOOPBACK ACTIVE 0-1 NEAR END LOOPBACK LTx TO LRx 1-0 DIGITAL LOOPBACK DSTi TO DSTo 1-1 REMOTE LOOPBACK LRx TO LTx
B5	FSync	IF '1', THE DEVICE WILL MAINTAIN FRAME SYNCHRONIZATION EVEN AFTER LOSING THE FRAMING SEQUENCE. IF '0', SYNCHRONIZATION WILL BE DECLARED WHEN 3 CONSECUTIVE FRAMING SEQUENCES HAVE BEEN DETECTED WITHOUT ERROR.
B4	FLv	IF '1', THE FRAME SYNC SEQUENCE WILL VIOLATE THE BIPOLAR VIOLATION ENCODING RULE. IF '0', THE FRAMING PATTERN RESUMES NORMAL OPERATIONS i.e. FRAMING BIT IS BIPOLAR VIOLATION.
B3	IDLE	SETTING THIS BIT TO '1' WILL FORCE AN ALL 0'S SIGNAL TO BE TRANSMITTED ON THE LINE.
B2	ECHO	SETTING THIS BIT TO '1' WILL FORCE ALL D-ECHO BITS (E) TO ZERO.
B1	SLAVE	IF '1', THE DEVICE WILL OPERATE IN A NT SLAVE MODE. THIS ALLOWS THE DEVICE TO BE USED AT THE TERMINAL EQUIPMENT END OF THE LINE WHILE RECEIVING ITS CLOCKS FROM AN EXTERNAL SOURCE.
B0	RegSel	IF THE REGISTER SELECT BIT IS SET TO '1', THE CONTROL REGISTER IS REDEFINED AS THE DIAGNOSTIC REGISTER. A '0' GIVES ACCESS TO THE CONTROL REGISTER.

Table A.12: NT mode status register - read address 01001b

BIT	NAME	DESCRIPTION
B7	SYNC/BA	THIS BIT IS SET WHEN THE DEVICE HAS ACHIEVED FRAME SYNCHRONIZATION WHILE THE ACTIVATION REQUEST IS ASSERTED (DR=0 AND AR=1). IF THERE IS A DEACTIVATION REQUEST OR AR IS LOW (DR=1 OR AR-0), THIS BIT INDICATES THE PRESENCE OF BUS ACTIVITY.
B6-B5	IS0-IS1	BINARY ENCODED STATE SEQUENCE: IS0-IS1 0 - 0 DEACTIVATED 1 - 0 PENDING ACTIVATION 0 - 1 PENDING DEACTIVATION 1 - 1 ACTIVATED
B4	RxMCH	THE STATE OF THIS BIT REFLECTS THE RECEIVED MAINTENANCE CHANNEL WHICH IS RECEIVED IN THE Fa BIT FOLLOWING THE MFR SIGNAL (Q-CHANNEL). THIS BIT WILL ALWAYS REMAIN ONE IF THE MFR SIGNAL IS NEVER ASSERTED.
B3-B0	NA	THESE BITS WILL READ '1'.